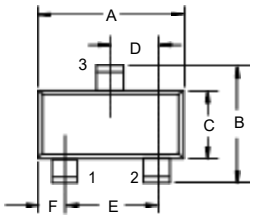
P-Channel Enhancement Mode Field Effect Transistor

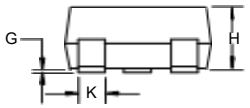
Features

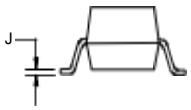
- -20V,-2.8A, $R_{DS(ON)}$=120mΩ@V_{GS}=-4.5V
  $R_{DS(ON)}$=150mΩ@V_{GS}=-2.5V
- High dense cell design for extremely low $R_{DS(ON)}$
- Rugged and reliable
- High Speed Switching
- SOT-23 Package
- Marking Code: 22P
- Epoxy meets UL 94 V-0 flammability rating
- Moisture Sensitivity Level 1

SOT-23



1.GATE
2. SOURCE
3. DRAIN



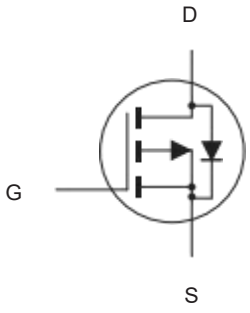


Maximum Ratings @ 25°C Unless Otherwise Specified

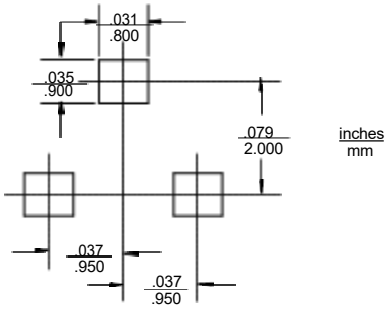
Symbol	Parameter	Rating	Unit
V_{DS}	Drain-source Voltage	-20	V
I_D	Drain Current-Continuous	-2.8	A
I_{DM}	Drain Current-Pulsed [a]	-10	A
V_{GS}	Gate-source Voltage	±8	V
P_D	Total Power Dissipation	1.25	W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient[b]	100	°C/W
T_J	Operating Junction Temperature	-55 to +150	°C
T_{STG}	Storage Temperature	-55 to +150	°C

DIMENSIONS					
	INCHES		MM		
DIM	MIN	MAX	MIN	MAX	NOTE
A	.110	.120	2.80	3.04	
B	.083	.098	2.10	2.64	
C	.047	.055	1.20	1.40	
D	.035	.041	.89	1.03	
E	.070	.081	1.78	2.05	
F	.018	.024	.45	.60	
G	.0005	.0039	.013	.100	
H	.035	.044	.89	1.12	
J	.003	.007	.085	.180	
K	.015	.020	.37	.51	

Internal Block Diagram



Suggested Solder Pad Layout



Electrical Characteristics T_A = 25 C unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V, I_D = -250μA	-20			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -20V, V_{GS} = 0V			-1	μA
Gate Body Leakage Current, Forward	I_{GSSF}	V_{GS} = 8V, V_{DS} = 0V			100	nA
Gate Body Leakage Current, Reverse	I_{GSSR}	V_{GS} = -8V, V_{DS} = 0V			-100	nA
On Characteristics[c]						
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}= V_{DS}, I_D = -250μA	-0.45			V
Static Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS} = -4.5V, I_D = -2.8A		80	120	mΩ
		V_{GS} = -2.5V, I_D = -2.0A		110	150	mΩ
Forward Transconductance	g_{FS}	V_{DS} = -5V, I_D = -2.8A		8		S
Dynamic Characteristics[d]						
Input Capacitance	C_{iss}	V_{DS} = -6V, V_{GS} = 0V, f = 1.0 MHz		880		pF
Output Capacitance	C_{oss}			270		pF
Reverse Transfer Capacitance	C_{rss}			175		pF
Switching Characteristics[d]						
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = -6V, I_D = -1A, V_{GS} = -4.5V, R_{GEN} =6Ω		11	20	ns
Turn-On Rise Time	t_r			5	10	ns
Turn-Off Delay Time	$t_{d(off)}$			32	65	ns
Turn-Off Fall Time	t_f			23	45	ns
Total Gate Charge	Q_g	V_{DS} = -6V, I_D = -2.8A, V_{GS} = -4.5V		11	14.5	nC
Gate-Source Charge	Q_{gs}			1.5		nC
Gate-Drain Charge	Q_{gd}			2.1		nC
Drain-Source Diode Characteristics and Maximun Ratings						
Drain-Source Diode Forward Current[b]	I_S				-0.75	A
Drain-Source Diode Forward Voltage[c]	V_{SD}	V_{GS} = 0V, I_S = -0.75A			-1.2	V

Notes :
a.Repetitive Rating : Pulse width limited by maximum junction temperature.
b.Surface Mounted on FR4 Board, t < 5 sec.
c.Pulse Test : Pulse Width < 300μs, Duty Cycle < 2%.
d.Guaranteed by design, not subject to production testing.

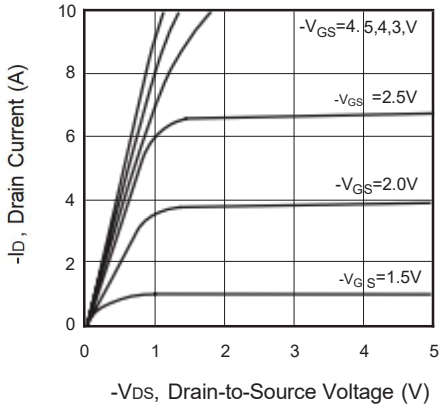


Figure 1. Output Characteristics

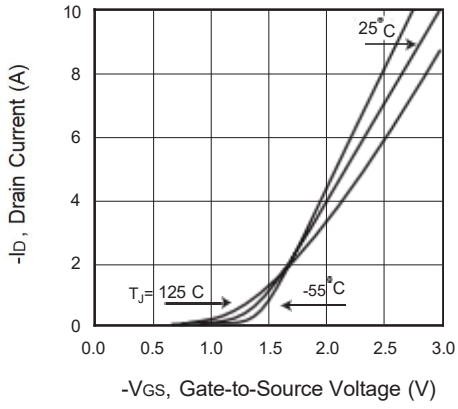


Figure 2. Transfer Characteristics

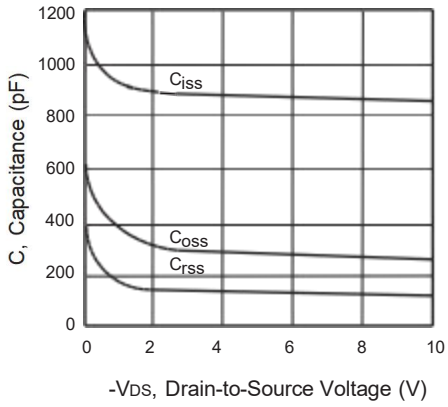


Figure 3. Capacitance

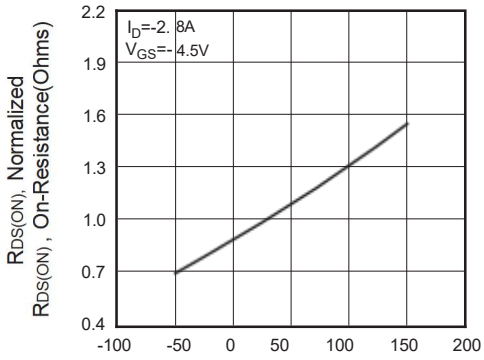


Figure 4. On-Resistance Variation with Temperature

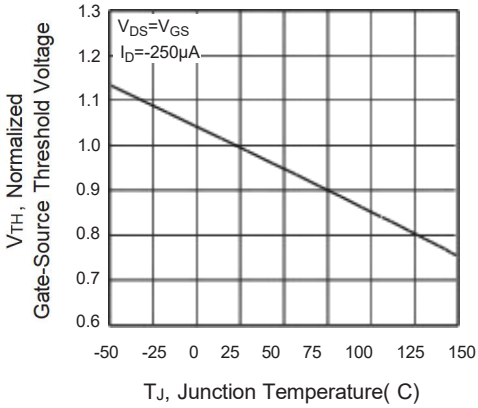


Figure 5. Gate Threshold Variation with Temperature

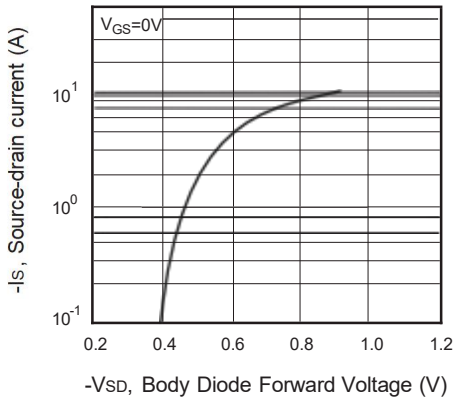


Figure 6. Body Diode Forward Voltage Variation with Source Current

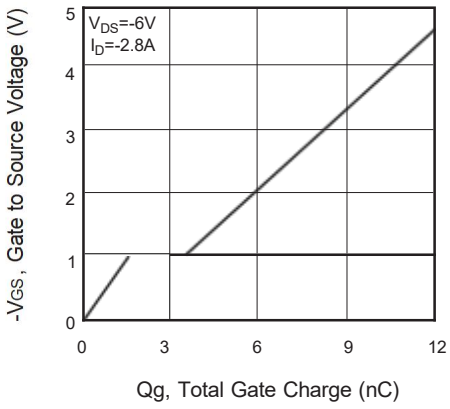


Figure 7. Gate Charge

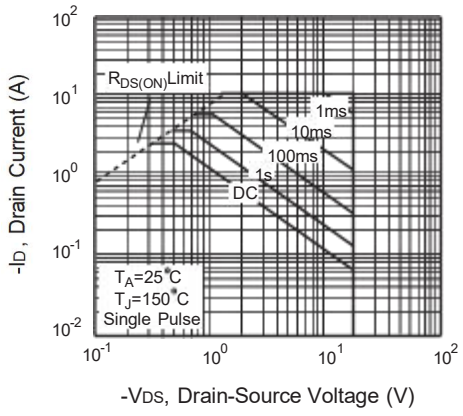


Figure 8. Maximum Safe Operating Area

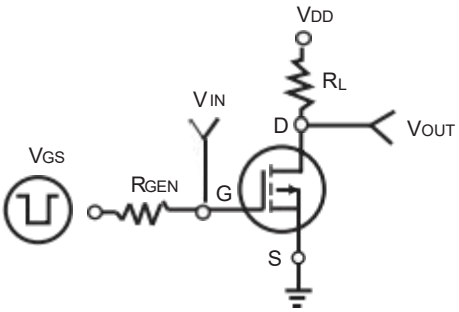


Figure 9. Switching Test Circuit

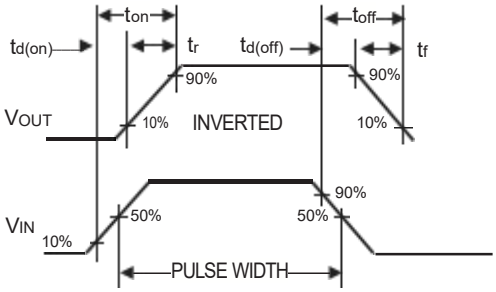


Figure 10. Switching Waveforms

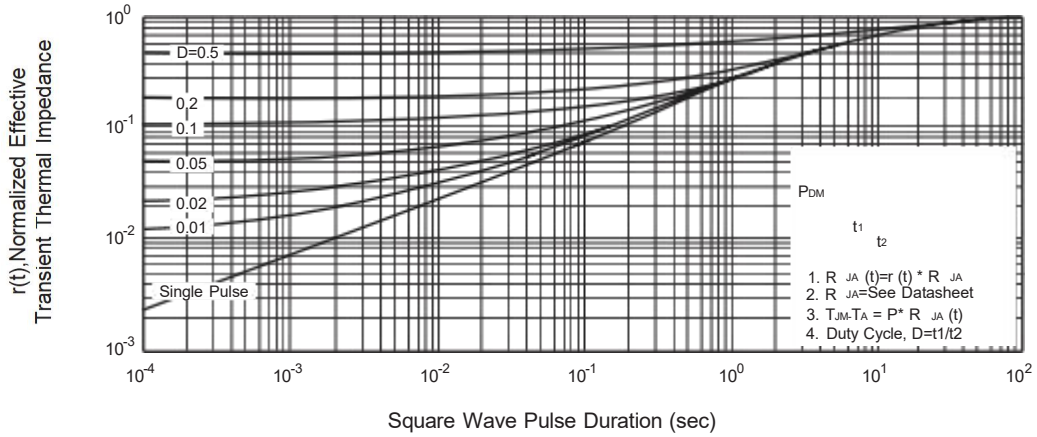


Figure 11. Normalized Thermal Transient Impedance Curve